REMARKS/ARGUMENTS

Status of claims

Claim 1 is pending and at issue. Claims 2 and 3 have been withdrawn.

Election / Restriction

The Examiner's acknowledgment of applicants' election of claim 1 is hereby noted.

Descriptive summary of the invention

Before discussing the cited prior art and the Examiner's rejections of the claims in view of that art, it would be appropriate to present a brief summary of applicant's invention. This summary is based on the specification. It is provided only for the convenience of the Examiner, and is not intended to argue limitations which are unclaimed. Many semiconductor devices, including integrated circuits (ICs), very large scale integrated circuits (VLSIs) and transistor arrays, are formed using a semiconductor base board fabricated from a silicon wafer. It is necessary to form one or more conductive bumps on the semiconductor base board so as to enable connection of electrical terminal leads to the semiconductor device. Conductive bumps are created by forming a pad on the silicon base board, forming a metal plating layer over the pad, compressing one or more metal solder balls to the metal plating layer, and melting the solder balls. Alternatively, conductive bumps may be formed by printing a metal paste on the silicon base board, or by connecting a wire bonding to the silicon base board.

The formed conductive bumps may cause a crack to form on the semiconductor base board in subsequent processing steps. This problem is exacerbated by the current trend to use thinner and smaller semiconductor wafers to provide improved operation at higher frequencies. As the

thickness of a semiconductor wafer decreases, crack formation becomes an ever greater concern. Accordingly, the device disclosed in the present application solves the wafer cracking problem by removing a breakable layer on the principal surface to expose a crystalline layer which is disposed innermore than the breakable layer. After the crystalline layer is exposed, bumps are formed on a predetermined position on the other principal surface of the semiconductor base board. The foregoing features are advantageous in preventing the formation of cracks on the semiconductor base board due to applied stress during bump formation.

The breakable layer and the crystalline layer are described in greater detail at page 9, line 16 to page 10, line 8 of the present specification, and are illustrated in FIG. 3. More specifically, when the back surface of a silicon wafer has been subjected to a grinding operation, this creates a multi-layer structure in which a breakable layer 31 (FIG. 3) and a crystalline layer 32 are formed. Breakable layer 31 extends from the back surface to about 30 micrometers inward from the back surface. Crystalline layer 32 starts at a depth of at least 30 micrometers inward from the back surface and extends to greater depths. Micro-cracks 18 may form in breakable layer 31, but such cracks do not form in crystalline layer 32. By mirror-finishing the ground back surface of the silicon wafer to a 1-30 micrometer depth, the micro-crack containing breakable layer 31 is removed to expose a crystalline layer 32 that does not contain any micro-cracks.

Patentability of claim 1 over U.S. Patent No. 6,506,681

The Examiner rejected claim 1 under 35 USC 102(a) as being anticipated by Grigg et al., U.S. Patent No. 6,506,681. According to the Examiner, FIG. 2B of Grigg discloses a thin flip chip where a semiconductor baseboard 10 is ground, thinning the baseboard to remove a thickness 17a, and bumps 18 are located on the other surface of the baseboard. However, Grigg fails to disclose removal of "a breakable layer on the principal surface" to expose "a crystalline layer which is

disposed innermore than the breakable layer". This feature, explicitly set forth in claim 1, is neither disclosed in, nor suggested by, the Grigg patent. The claimed feature prevents a crack from forming on the semiconductor baseboard due to applied stress from processing steps that are performed subsequent to a bump forming operation.

Although Grigg also deals with applied stress subsequent to a bump-forming operation, the manner in which Grigg deals with this stress is completely distinguishable from applicant's invention as set forth in claim 1. With reference to col. 6, line 58- col. 7, line 4 of Grigg, "according to the methods of the present invention, a mold compound is placed on the active surface area of the semiconductor wafer to provide support and protection for the semiconductor wafer structure, both during and after a process of removing the surface of inactive backside of the semiconductor wafer. The mold compound also serves to preserve the integrity of the conductively bumped aspects of the semiconductor wafer during subsequent processing, and may, after the semiconductor wafer is diced, act as all or part of an underfill material". In contrast to Grigg's approach, applicant's invention does not utilize a mold compound to protect and support formed conductive bumps.

Conclusion

Grigg fails to disclose or suggest applicant's claimed removal of "a breakable layer on the principal surface" to expose "a crystalline layer which is disposed innermore than the breakable layer". Moreover, Grigg uses a mold compound to deal with applied stress subsequent to a bump-forming operation, and this technique is completely distinguishable from applicant's invention as set forth in claim 1. Accordingly, it is submitted that claim 1 is neither anticipated by, nor rendered

obvious in view of, the Grigg patent. It is further submitted that claim 1 is allowable over the prior art of record, and such action by the Examiner is earnestly solicited.

Respectfully submitted,

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Dated: October 18, 2004